

EMC Modelling and Optimization for Reducing Capacitances of Interconnections with Arbitrary Shape in Multilayer VLSI Circuits

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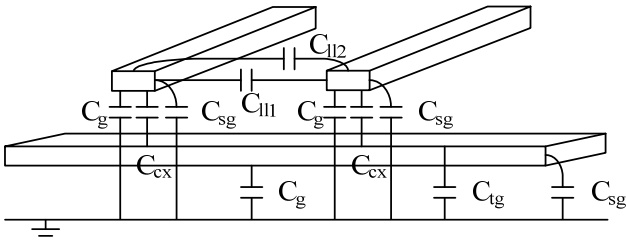
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Abstract—This paper presents an EMC modelling method for the purpose of calculating the interconnect capacitance between VLSI interconnects based on the finite element method (FEM). Two- and three-dimensional interconnect models are simulated and results of capacitance extraction are compared with experimental measurement which proved the consistency and accuracy of FEM. Furthermore, non-dominated sorting genetic algorithm II (NSGA-II) is applied for optimizations of two- and three-dimensional multilayer interconnection structures in order to obtain reduced interconnect coupling capacitances. The results show NSGA-II has a good capacity of optimization in multiobject. Both modelling and optimization methods are applicable to arbitrary interconnect structures in VLSI.

I. INTRODUCTION

Due to the exponential increases in transistors per chip, the interconnect power dissipation turns out dynamically in total percentage of power consumption [1]. The reason is that faster switching activities of interconnect capacitances with larger amount of interconnects bring huge consumption. Crosstalk is another issue that should be considered within shrinking chip size, which is related to not only large quantities of interconnects, but also multiple metallization layers and complex materials [2]. From an example of capacitance components of interconnect in Fig. 1, they are generally sorted into ground capacitance and coupling capacitance. Increasing ground capacitance and reducing coupling capacitance will benefit internal EMC phenomenon of VLSI circuit. To date, capacitance calculation of interconnect is inefficient. Therefore, an accurate and fast modelling approach of interconnects for electronic devices is becoming more significant for calculating interconnect capacitance in early design phases.



C_g, C_{tg}, C_{sg} : Ground Capacitance
 C_{ll1}, C_{ll2}, C_{cx} : Coupling Capacitance

Fig. 1 Example of interconnect capacitance

II. THEORETICAL BACKGROUND

A. Capacitance Calculation Methodology

There is a more accurate and faster method of calculation is to apply the principle of energy conservation using electrical field energy stored in the volume V . The electrostatic energy of a linear N electrode (the N^{th} is ground) system is:

$$W = \frac{1}{2} \sum_{i=1}^N C_{ii}^g V_i^2 + \frac{1}{2} \sum_{i=1, j=1, i \neq j}^N C_{ij}^g V_i V_j \quad (1)$$

where, W is electrostatic energy; V_i or V_j is the potential of i^{th} electrode with respect to the ground; C_{ii}^g is the self ground capacitance of i^{th} electrode and C_{ij}^g ($i \neq j$) is the mutual ground capacitance between electrodes. By applying appropriate voltages on electrodes, the coefficients of the ground capacitance can be calculated by using FEM from the stored static energy.

B. Optimization Algorithm - NSGA-II

As an improved version of nondominated sorting genetic algorithm (NSGA), NSGA-II performs a fast multiobjective evolution in terms of finding a diverse set of solutions and in converging near the true Pareto-optimal set [3]. The main procedure is described by a flow chart as shown in Fig. 2. More details of this algorithm will be introduced in the full paper.

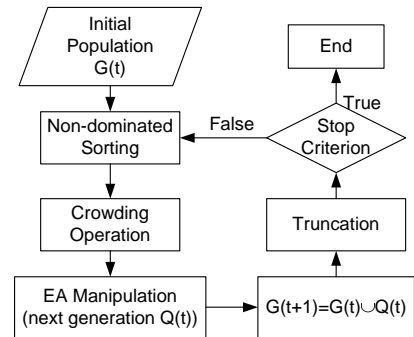


Fig. 2 A flow chart of NSGA-II process

III. SIMULATION AND OPTIMIZATION

A. Simulation and Verification

Figure 3 presents some typical interconnect structures, such as different interconnects wiring in two-dimension parallel and overlapping structures, and three-dimension crossover structure.

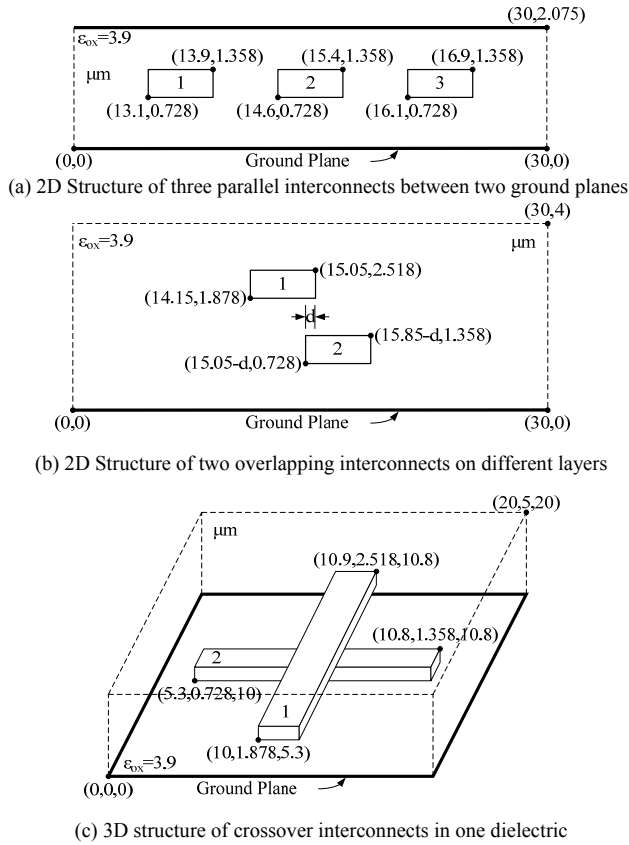


Fig. 3. Structure of different interconnects wiring

As listed in Table I, the capacitance of interconnect is calculated and compared with relative numerical and measurement results from Wong et al. [4]. For the parallel structure in Fig. 3 (a), the self capacitance of conductor 2 is used for comparison. For the overlapping structure in Fig. 3 (b), when distance $0 > d > -1.8$, the two interconnects overlap. Also, the self capacitance of conductor 1 in Fig. 3 (c) is used for comparison. FEM is proved correct and leads to a more accurate result. This result shows that FEM gives around 10% closer to the measurement comparing with semi-empirical model. More complicated 3D models will be offered in the full paper by comparison with [5].

Table I. Experimental results of different interconnects wiring

Structure/ (fF/ μ m)	Semi-empirical Model [4] & Accuracy vs Measurement	FEM & Accuracy vs Measurement (This paper)	Measur- ement [4]
(a)	0.216 (-7.9%)	0.214 (-8.9%)	0.233
(b) d=0	0.121 (+15.2%)	0.119 (+11.8%)	0.105
(b) d=0.4	0.136 (+11.8%)	0.132 (+10.0%)	0.120
(b) d=0.8	0.146 (+14.1%)	0.139 (+8.5%)	0.128
(b) d=-0.4	0.116 (+25.9%)	0.107 (+19.6%)	0.086
(c)	0.736 (-11.1%)	0.8044 (-1.7%)	0.818

B. Optimization

By the NSGA-II algorithm, an optimized capacitance result of interconnects can be obtained. For example of overlapping structure in Fig. 3 (b), optimization is needed on the coupling capacitance ($d=0.8$) between conductor 1 and 2 which are constrained within Layer1 and Layer2. From the optimized result in Fig. 4, it is found that coupling capacitance C12 or C21 reduced from $-0.93111E-16$ F to $-0.19336E-19$ F per unit length (in μ m).

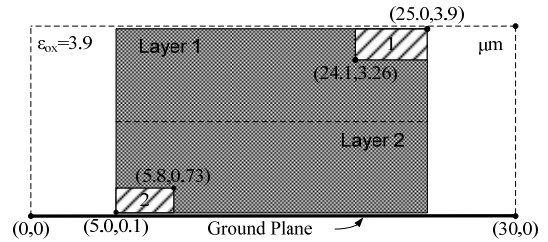


Fig. 4 Capacitance optimization of overlapping interconnects

The following Fig. 5 shows a complex 2D multilayer interconnect structure on different layers. Full optimization results and analysis will be presented in the full paper, as well as 3D model optimizations.

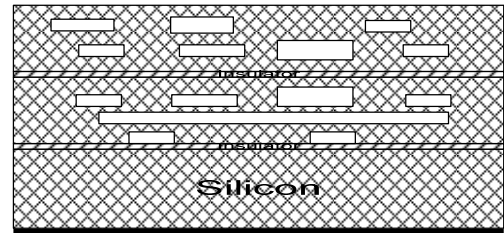


Fig. 5 2D multilayer interconnect on different layers for optimization

IV. CONCLUSION

In this paper, an EMC modelling approach is proposed to predict the capacitances by means of FEM within arbitrary shapes of VLSI interconnect structures. Optimization is done with help of NSGA-II in order to find better structure that reduce interconnect capacitances under certain restrictions. All the results are proved accurate.

V. REFERENCES

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